

257	349	
Class	Subclass	
		ISSUE CLASSIFICATION

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PATENT NUMBER

**U.S. UTILITY** Patent Application

<u>MR</u>	O.I.P.E.	PATENT DATE
SCANNED	NS 4 Q.A CTH	

APPLICATION NO. 09/865929	CONT/PRIOR D	CLASS 257	SUBCLASS 312	ART UNIT 2811 2811	EXAMINER IC AWS
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Min-hwa Chi

Transistor and logic circuit on thin silicon-on-insulator wafers  
based on gate induced drain leakage currents

## APPlicants

**TITLE**

## ISSUING CLASSIFICATION

Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> TERMINAL DISCLAIMER		<b>DRAWINGS</b> Sheets Drwg. <u>9</u> Figs. Drwg. <u>14</u> Print Fig. <u>10</u>			<b>CLAIMS ALLOWED</b> Total Claims <u>8</u> Print Claim for O.G. <u>1</u>	
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.						
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____		<i>Karen Alan</i> <u>5-12-03</u> (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b> <i>5/16/03</i>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.		<i>Steve Lake</i> <u>5/13/03</u> (Primary Examiner) (Date)			<b>ISSUE FEE</b> Amount Due <u>1600</u> Date Paid _____	
		<i>Wanda Collins</i> <u>5/22/03</u> (Legal Instrument Examiner) (Date)			<b>ISSUE BATCH NUMBER</b> _____	

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**(Rev. 6/99)**

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Illustrated in pencil on right side map.

(FACE)